In the Claims:

Please amend claims 1 and 20. The claims are as follows:

1. (Currently Amended) A CRC generator/checker for generating CRC results, comprising:

a set of CRC circuits connected in series, each CRC circuit responsive to a different control signal generated by a control logic, each CRC circuit having a seed input adapted to receive a seed [[,]] ;

a data input adapted to receive and process a different set of M-bits of a data unit and a result output adapted to generate a result, the result output of a previous CRC circuit connected to the seed input of an immediately subsequent CRC circuit, the seed input of a first CRC circuit connected to an output of a remainder register[[,]]; and

an input of said remainder register connected to an output of a multiplexer, the result outputs of said ~~multiplicity~~ set of CRC circuits connected to different inputs of said multiplexer, said multiplexer responsive to a select signal generated by said control logic.

2. (Original) The CRC generator/checker of claim 1, wherein said control logic is adapted to generate said select signal based on the bit width of said data unit, said control signals causing a particular CRC circuit to generate a result based on a particular set of M-bits and the result of a previous CRC circuit or the contents of said remainder register if the particular CRC circuit is said first CRC circuit, or based on the particular set of M-bits or the contents of said remainder register if the particular CRC circuit is said first CRC circuit and an internally generated seed.

3. (Original) The CRC generator/checker of claim 1, wherein a number of said CRC circuits is equal to the highest integer not exceeding the width in bits of a data bus supplying said data unit divided by M.

4. (Original) The CRC generator/checker of claim 1, wherein M is 8.

5. (Original) The CRC generator/checker of claim 1, wherein M=8 and further including:

a set of multi-byte CRC circuits, each multi-byte CRC circuit adapted to simultaneously process a multiple number of bytes of said data unit;

each multi-byte CRC circuit responsive to a different additional control signal generated by said control logic, each multi-byte CRC circuit having a seed input adapted to receive a seed selectable from said remainder register, all result outputs of said CRC circuits and the result outputs from all higher byte number multi-byte CRC circuits, a data input adapted to receive said multiple number bytes of data and a result output adapted to generate a result, the result output of each multi-byte CRC circuit connected to different additional inputs of said multiplexer; and

said additional control signals causing a particular multi-byte CRC circuit to generate a result based on multiple byte data and said selectable seed or based on said multiple-byte data and an internally generated seed.

6. (Original) The CRC generator/checker of claim 5, wherein:

each multi-byte CRC is adapted to process a different number of bytes of data selected from the series of powers of two bytes in the range 2^(N-1) to 2^Y where 2^(N-1) is equal to a number of said CRC circuits in said set of CRC circuits and Y is less than (N-1); and

wherein Y is chosen such the number of concatenated multi-byte CRC calculations performed plus {W-[2^(N-1)+2^(N=2)+...+2^Y]} concatenated 1-byte CRC calculations can be performed in a single clock cycle and where W is the width in bytes of a data bus supplying said data unit and the number of CRC circuits.

7. (Original) The CRC generator/checker of claim 6, further including a total of Q identical multi-byte CRC circuits selected from said set of multi-byte circuits wherein the Q identical multi-byte CRC circuits are adapted to process (2^X)-bytes of data where X is defined by (2^X) ≤ L and 2^(X+1)>L where L is a maximum number of 1-byte concatenated CRC calculations that can be done by said CRC circuits in a single clock cycle, and Q is defined by the largest integer not exceeding |W/(L+1)| where and where W is the width in bytes of a data bus supplying said data unit and the number of CRC circuits.

8. (Original) The CRC generator/checker of claim 7, wherein:

a subset of CRC circuits comprising the last (W-L) CRC circuits of said multiplicity of CRC circuits have seed inputs adapted to receive a seed selectable from an immediately previous CRC circuit and the result outputs of all of said multi-byte CRC circuits, the output result of each CRC circuit of said subset of CRC circuits based on said selectable seed and a corresponding byte of data or based on an internally generated seed and said corresponding byte of data.

9. (Original) The CRC generator/checker of claim 8, wherein W=32, L=10, N=5, X=3, Y=2 and Q=2.

10. (Original) The CRC generator/checker of claim 8, wherein said CRC result is generated in one clock cycle.

11. (Original) The CRC generator/checker of claim 1, wherein the number of CRC circuits is scalable to a width of said data bus.

12. (Original) A CRC generator/checker, comprising:

a multiplicity of CRC circuits adapted to process a single-byte of data from a data bus, each CRC circuit having a seed input, a data input adapted to receive a different byte of data from said bus, a control input and a result output;

an multiplexer having an output connected to an input of a remainder register, a select input and a multiplicity of inputs, each result output of each said CRC circuit connected to a different input of said multiplexer;

each CRC circuit connected in series, the result output of a previous CRC circuit connected to the seed input of an immediately subsequent CRC circuit, the seed input of a first CRC circuit connected to an output of said remainder register; and

a control logic having a select output and a multiplicity of control outputs, said select output connected to said select input of said multiplexer and said control outputs connected to corresponding control inputs of said CRC circuits.

13. (Original) The CRC generator/checker of claim 12, further including:

a set of multi-byte CRC circuits, each having a seed input, a control input and a result output connected to different additional inputs of said multiplexer and each multi-byte circuit adapted to simultaneously process a multiple number of bytes of data;

each multi-byte CRC circuit responsive to a different additional control signal generated by said control logic, the seed input of each multi-byte CRC circuit adapted to receive a selectable seed selectable from all result outputs of said CRC circuits and the result outputs from any higher-byte number multi-byte CRC circuit, the data input of each multi-byte CRC circuit adapted to receive a different set of multi-bytes of said, the result output of each multi-byte CRC circuit; and

said additional control signals causing a particular multi-byte CRC circuit to generate a result based on a corresponding multiple bytes of said data and said selectable seed or based on said corresponding multi-bytes of said data and an internally generated seed.

14. CRC generator/checker of claim 13, wherein:

each multi-byte CRC is adapted to process a different number of bytes of data selected from the series of powers of two bytes in the range 2^(N-1) to 2^Y where 2^(N-1) is equal to a number of said CRC circuits in said set of CRC circuits and Y is less than (N-1); and

wherein Y is chosen such the number of concatenated multi-byte CRC calculations performed plus {W-{2^(N-1)+2(N-2)+...+2^Y]} concatenated 1-byte CRC calculations can be performed in a single clock cycle and where W is the width in bytes of said data bus and the number of CRC circuits.

15. (Original) The CRC generator/checker of claim 14, further including a total of Q identical multi-byte CRC circuits selected from said set of multi-byte circuits wherein the Q identical multi-byte CRC circuits are adapted to process (2^X)-bytes of data where X is defined by (2^X) ≤ L and 2^(X+1)>L where L is a maximum number of 1-byte concatenated CRC calculations that can be done by said CRC circuits in a single clock cycle, and Q is defined by the largest

integer not exceeding |W/(L+1)| and where W is the width in bytes of said data bus and the number of CRC circuits.

16. (Original) The CRC generator/checker of claim 15, wherein:

a subset of CRC circuits comprising the last (W-L) CRC circuits of said multiplicity of CRC circuits have seed inputs adapted to receive a seed selectable from an immediately previous CRC circuit and the result outputs of all of said multi-byte CRC circuits, the output result of each CRC circuit of said subset of CRC circuits based on said selectable seed and a corresponding byte of data or based on an internally generated seed and said corresponding byte of data.

17. (Original) The CRC generator/checker of claim 16, wherein W=32, L=10, N=5, X=3, Y=2 and Q=2.

18. (Original) The CRC generator/checker of claim 16, wherein said CRC result is generated in one clock cycle.

19. (Original) The CRC generator/checker of claim 12, wherein the number of CRC circuits is scalable to a byte width of said data bus.

20. (Currently Amended) A method of generating and checking a CRC result, comprising:

providing a control circuit for generating control signals and a select signal;

providing a multiplexer; and

providing a set of CRC circuits connected in series, each CRC circuit responsive to a different control signal generated by a control logic, each CRC circuit having a seed input adapted to receive a seed[[,]];

providing a data input adapted to receive and process a different set of M-bits of a data unit and a result output adapted to generate a result, the result output of a previous CRC circuit connected to the seed input of an immediately subsequent CRC circuit, the seed input of a first CRC circuit connected to an output of a remainder register[[,]]; and

providing an input of said remainder register connected to an output of said multiplexer, the result outputs of said ~~multiplicity~~ set of CRC circuits connected to different inputs of said multiplexer, said multiplexer responsive to a select signal generated by said control logic.

21. (Original) The method of claim 20, further including:

generating said select signal based on the bit width of said data;

said control signals causing a particular CRC circuit to generate a result based on a particular set of M-bits and the result of a previous CRC circuit or the contents of said remainder register if the particular CRC circuit is said first CRC circuit, or based on the particular set of M-bits or the contents of said remainder register if the particular CRC circuit is said first CRC circuit and an internally generated seed.

22. (Original) The method of claim 20, wherein a number of said CRC circuits is equal to the highest integer not exceeding the width in bits of a data bus supplying said data unit divided by M.

23. (Original) The method of claim 20, wherein M is 8.

24. (Original) The method of claim 20, wherein M=8 and further including:

providing a set of multi-byte CRC circuits, each multi-byte CRC circuit adapted to simultaneously process a multiple number of bytes of said data unit;

each multi-byte CRC circuit responsive to a different additional control signal generated by said control logic, each multi-byte CRC circuit having a seed input adapted to receive a seed selectable from said remainder register, all result outputs of said CRC circuits and the result outputs from all higher byte number multi-byte CRC circuits, a data input adapted to receive said multiple number bytes of data and a result output adapted to generate a result, the result output of each multi-byte CRC circuit connected to different additional inputs of said multiplexer; and

said additional control signals causing a particular multi-byte CRC circuit to generate a result based on multiple byte and said selectable seed or based on said multiple-byte data and an internally generated seed.

25. (Original) The method of claim 24, wherein:

each multi-byte CRC is adapted to process a different number of bytes of data selected from the series of powers of two bytes in the range 2^(N-1) to 2^Y where 2^(N-1) is equal to a number of said CRC circuits in said set of CRC circuits and Y is less than (N-1); and

further including choosing Y such the number of concatenated multi-byte CRC calculations performed plus {W-[2^(N-1)+2^(N=2)+...+2^Y]} concatenated 1-byte CRC calculations can be performed in a single clock cycle and where W is the width in bytes of a data bus supplying said data unit and the number of CRC circuits.

26. (Original) The method of claim 25, further including providing a total of Q identical multi-byte CRC circuits selected from said set of multi-byte circuits wherein the Q identical multi-byte CRC circuits are adapted to process (2^X)-bytes of data where X is defined by (2^X) ≤ L and 2^(X+1)>L where L is a maximum number of 1-byte concatenated CRC calculations that can be done by said CRC circuits in a single clock cycle, and Q is defined by the largest integer not exceeding |W/(L+1)| and where W is the width in bytes of a data bus supplying said data unit and the number of CRC circuits.

27. (Original) The method of claim 26, wherein:

providing a subset of CRC circuits, said subset of CRC circuits comprising the last (W-L) CRC circuits of said multiplicity of CRC circuits and having seed inputs adapted to receive a seed selectable from an immediately previous CRC circuit and the result outputs of all of said multi-byte CRC circuits, the output result of each CRC circuit of said subset of CRC circuits based on said selectable seed and a corresponding byte of data of said data or based on an internally generated seed and said corresponding byte of data of said data.

28. (Original) The CRC generator/checker of claim 26, wherein W=32, L=10, N=5, X=3, Y=2 and Q=2.

29. (Original) The method of claim 26, wherein said CRC result is generated in one clock cycle.

30. (Original) The method of claim 20, wherein the number of CRC circuits is scalable to a width of said data bus.